	L #	Hits	Search Text	DBs	Time Stamp
1	L1	56	("PLL" or phase adj2 loop) and operat$3 near2 stop$4 near2 detect$4	USPAT; EPO; JPO; DERWENT	2003/05/13 10:54
2	L2	565	("PLL" or phase adj2 loop) and operat$3 with stop$4 with detect$4	USPAT; EPO; JPO; DERWENT	2003/05/13 10:55
3	L3	509	2 not 1	USPAT; EPO; JPO; DERWENT	2003/05/13 10:55
4	L4	92	3 and (327/$.ccls. or 331/$.ccls. or 375/$.ccls.)	USPAT; EPO; JPO; DERWENT	2003/05/13 13:11
5	L5	1	"11122102"	JPO	2003/05/13 11:35
6	L6	0	"0107627"	JPO	2003/05/13 11:36
7	L7	1	"10107627"	JPO	2003/05/13 11:36
8	L8	1	"06338786"	JPO	2003/05/13 11:36
9	L9	15	("PLL" or phase adj2 loop) and (327/$.ccls. or 331/$.ccls. or 375/$.ccls.) and (dead adj lock or deadlock)	USPAT; EPO; JPO; DERWENT	2003/05/13 13:12

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703-308-4922

PAT-NO: JP410107627A

DOCUMENT-IDENTIFIER: JP 10107627 A

TITLE: PHASE-LOCKED LOOP CIRCUIT

PUBN-DATE: April 24, 1998

INVENTOR-INFORMATION:
NAME
TAKADA, MASATOSHI

ASSIGNEE-INFORMATION:
NAME COUNTRY
KAWASAKI STEEL CORP N/A

APPL-NO: JP08260455

APPL-DATE: October 1, 1996

INT-CL (IPC): H03L007/10, H03L007/093

ABSTRACT:

PROBLEM TO BE SOLVED: To detect falling into a deadlock state and to automatically recover to a normal state by detecting that a PLL circuit reaches
certain voltage or more where there is possibility that it falls into a deadlock state through the voltage level of a control signal and reducing the

SOLUTION: A feedback signal is inputted from a logic circuit 22 to a phase
comparator 12 and a deadlock detecting circuit 24. The detecting circuit 24 considers that the PLL circuit 10 enters a deadlock state and outputs a high-level detection signal if the feedback signal has transition and no clear signal is outputted from the rise to the fall of a frequency division signal as a reference signal. A control signal control circuit 14 controls control signals UP1 and DOWN1 according to the detection signal outputted from the
detecting circuit 24 so that the control signal outputted from the detecting circuit 24 drops in voltage level and outputs control signals UP2 and DOWN2 for
controlling a charge pump 16.

PAT-NO: JP411122102A

DOCUMENT-IDENTIFIER: JP 11122102 A

TITLE: PLL CIRCUIT

PUBN-DATE: April 30, 1999

INVENTOR-INFORMATION:
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KAWASAKI STEEL CORP N/A

APPL-NO: JP09280218

APPL-DATE: October 14, 1997

INT-CL (IPC): H03L007/12

ABSTRACT:

PROBLEM TO BE SOLVED: To make automatic recovery to a normal lock state even
if a deadlock state is entered by detecting the deadlock state being entered and controlling control signals so that the voltage level of a control signal drops.

PURPOSE: To prevent the dead lock of a frequency divider from occurring by
discharging a charge/discharge circuit compulsorily via a gate on the discharge
path of the charge/discharge circuit corresponding to the reset voltage of a microcomputer or the detection voltage of a detection circuit when a frequency
dividing operation is stopped.

CONSTITUTION: When the microcomputer is reset first, a reset voltage RST of
high level is applied to the control terminal of a transmission gate 9 via an OR gate 16, which forms the discharge path of the charge/discharge circuit. An
electric charge accumulated in a capacitor 6 is discharged compulsorily by a time constant T via a pull-down resistor 10. Therefore, a control voltage Vs can be decreased to around 0V when the microcomputer is reset, which surely
prevents the dead lock of the frequency divider 7 from occurring. Also, such state where the dead lock occurs due to infeasibility to follow up the oscillation clock of an oscillation frequency of extremely high level by the frequency divider 7 when the microcomputer is being operated normally can be
surely released even when it occurs.

PAT-NO: JP406338786A

DOCUMENT-IDENTIFIER: JP 06338786 A

TITLE: MICROCOMPUTER

PUBN-DATE: December 6, 1994

INVENTOR-INFORMATION:
NAME
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CHIAKI, KAZUMASA
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ASSIGNEE-INFORMATION:
NAME COUNTRY
SANYO ELECTRIC CO LTD N/A

APPL-NO: JP05129444

APPL-DATE: May 31, 1993

INT-CL (IPC): H03L007/089, G06F001/04 , G06F015/78

US-CL-CURRENT: 331/108R

ABSTRACT:

voltage level of the control signal.

SOLUTION: A control signal, etc., which is outputted from a low-pass filter
16 is inputted to a control circuit 20. The circuit 20 detects a voltage level of a control signal and detects whether or not a PLL circuit 10 is in a deadlock state. If the circuit 10 is in a deadlock state, the circuit 20 outputs a detection signal which is in an active state to recover it into a normal locked state. That is, the voltage level of a control signal detects that the circuit 10 reaches certain voltage level or more where there is possibility that it falls into a deadlock state and further, that it is in a deadlock state, and reduces the voltage level of the control signal.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-107627
(43)Date of publication of application : 24.04.1998

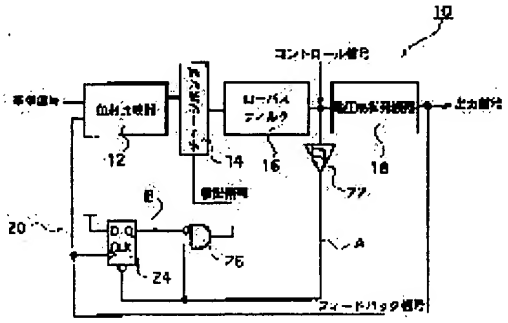
(51)Int.CI. H03L 7/10
H03L 7/093

(21)Application number : 08-260455
(22)Date of filing : 01.10.1996

(71)Applicant : KAWASAKI STEEL CORP
(72)Inventor : TAKADA MASATOSHI

(54) PHASE-LOCKED LOOP CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To detect falling into a deadlock state and to automatically recover to a normal state by detecting that a PLL circuit reaches certain voltage or more where there is possibility that it falls into a deadlock state through the voltage level of a control signal and reducing the voltage level of the control signal.
SOLUTION: A control signal, etc., which is outputted from a low-pass filter 16 is inputted to a control circuit 20. The circuit 20 detects a voltage level of a control signal and detects whether or not a PLL circuit 10 is in a deadlock state. If the circuit 10 is in a deadlock state, the circuit 20 outputs a detection signal which is in an active state to recover it into a normal locked state. That is, the voltage level of a control signal detects that the circuit 10 reaches certain voltage level or more where there is possibility that it falls into a deadlock state and further, that it is in a deadlock state, and reduces the voltage level of the control signal.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The phase comparator which detects the phase contrast between the reference signals and feedback signals which are characterized by providing the following, and outputs a control signal, The charge pump which outputs the error signal which has the pulse width according to the phase contrast between the aforementioned reference signal and a feedback signal according to the aforementioned control signal, The PLL circuit which has the low pass filter which outputs the control signal which has a voltage level according to the aforementioned error signal, and the voltage controlled oscillator which outputs the aforementioned feedback signal with which oscillation frequency was changed according to the voltage level of the aforementioned control signal. Furthermore, the 1st detection means which detects that the aforementioned control signal is more than a predetermined voltage level. The 2nd detection means which detects that the aforementioned feedback signal is not oscillating when it is detected by this 1st detection means that the aforementioned control signal is more than a predetermined voltage level. The 3rd detection means which outputs the detecting signal for lowering the voltage level of the aforementioned control signal when it is detected by this 2nd detection means that the aforementioned feedback signal is not oscillating.
[Claim 2] It is the PLL circuit according to claim 1 which the aforementioned detecting signal is inputted into the aforementioned charge pump, and is characterized by the aforementioned charge pump outputting the aforementioned error signal for lowering the voltage level of the aforementioned control signal according to the aforementioned detecting signal.
[Claim 3] The PLL circuit which is a PLL circuit according to claim 1, and is characterized by having further the means which lowers the voltage level of the aforementioned control signal according to the aforementioned detecting signal.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the PLL circuit (Phase-Locked Loop : phase synchronous loop) which generates the output signal by which phase simulation was carried out to the reference signal.
[0002]
[Description of the Prior Art] Drawing 4 is the conceptual diagram of an example showing the internal configuration of a PLL circuit. The PLL circuit 30 of the example of illustration is constituted by the voltage controlled oscillator 38 which outputs a feedback signal and an output signal according to the voltage level of the phase comparator 32 which compares the phase of a reference signal and a feedback signal and outputs a control signal, the charge pump 34 which outputs an error signal according to a control signal, the low pass filter 36 which outputs the control signal which has a voltage level according to the error signal, and a control signal.
[0003] In this PLL circuit 30, in a phase comparator 32, the phase contrast between a reference signal and a feedback signal is detected, and the control signal which it is as a result of [the] comparison is outputted. An error signal is generated based on a control signal, after an error signal is changed into an analog signal by the low pass filter 36, it is inputted into a voltage controlled oscillator 38 as a control signal by the charge pump 34, and the oscillation frequency of a feedback signal is changed in a voltage controlled oscillator 38 with it according to the voltage level of this control signal.
[0004] For example, when the phase of a feedback signal is later, in order to carry out the phase of a feedback signal early to a reference signal, it is made high, and the voltage level of a control signal is conversely made low in a voltage level, when early. And by repeating and detecting similarly hereafter the phase contrast between a reference signal and the feedback signal with which oscillation frequency was changed, the frequency and the phase between a reference signal and a feedback signal were synchronized (lock), and the output signal has been obtained.
[0005] Thus, in the PLL circuit 30, the frequency and the phase of a feedback signal were controlled by the voltage level of a control signal, and the output signal with which the phase of a reference signal and a feedback signal synchronized has been obtained by it.
[0006] By the way, the above-mentioned PLL circuit 30 is carried in individual ICs, such as a control unit, a processor, and CPU, turns on chip, and it is not only IC-ized alone, but may be used for the clock control etc. In this case, if various conditions, such as voltage variation, and temperature change, process change, are taken into consideration, it is necessary to design a voltage controlled oscillator 38 with sufficient margin so that it can operate from low frequency to high frequency focusing on the oscillation frequency used.
[0007] Thus, in IC in which the PLL circuit 30 designed with sufficient margin for the oscillation

frequency of a voltage controlled oscillator 38 is carried, a voltage controlled oscillator 38 can be oscillated to very high frequency rather than the real frequency of operation when actually operating IC. For example, though it does not oscillate to so high frequency at the time of worst conditions, at the time of best conditions, the maximum oscillation frequency of a voltage controlled oscillator 38 turns into typical conditions and very high frequency further.

[0008] By the way, circuit elements, such as a logic gate and a flip-flop, are usually connected to the path of a feedback signal. However, if the operating state of the PLL circuit 30 becomes unstable, the voltage level of a control signal goes up and the oscillation frequency of a voltage controlled oscillator 38 becomes high, it becomes impossible for one on the path of a feedback signal of circuit elements to toggle on the oscillation frequency of a voltage controlled oscillator 38, and a feedback signal may not no longer be inputted into a phase comparator 32.

[0009] If a feedback signal is no longer inputted into a phase comparator 32, it will judge that the phase comparator 32 is behind a reference signal in a feedback signal, and the control signal for making high further oscillation frequency of a voltage controlled oscillator 38 will be outputted. thus, the voltage level of a control signal goes up further -- having -- just -- being alike -- it changes a stack into a state with a high voltage level, and lapses into the deadlock state where the oscillation frequency of a voltage controlled oscillator 38 is fixed to an oscillation upper limited frequency

[0010] However, if the PLL circuit 30 did not initialize making a power supply into an OFF state, for example etc. once it lapsed into the deadlock state, it was difficult for constituting the PLL circuit system which could not be returned to a normal lock state and stabilized.

[0011] Therefore, in IC in which the PLL circuit 30 was carried, in order to avoid a deadlock state beforehand, in consideration of the upper limited frequency of the path of a feedback signal of operation, you have to design so that it can operate to frequency very higher than the real frequency of operation of IC. When the PLL circuit 30 was especially used for clock control, the restrictions on a design -- the path of a clock signal must enable it to operate to frequency very higher than a real frequency of operation, and the restrictions to the load of the path of a clock signal become severe -- increased, and there was a trouble that a design became very difficult.

[0012]

[Problem(s) to be Solved by the Invention] The purpose of this invention tries to return the trouble based on the aforementioned conventional technology, detects having lapsed into the deadlock state, and is to offer the PLL circuit which can return to a normal state automatically.

[0013]

[Means for Solving the Problem] The phase comparator which this invention detects the phase contrast between a reference signal and a feedback signal, and outputs a control signal in order to attain the above-mentioned purpose, The charge pump which outputs the error signal which has the pulse width according to the phase contrast between the aforementioned reference signal and a feedback signal according to the aforementioned control signal, The low pass filter which outputs the control signal which has a voltage level according to the aforementioned error signal, It is the PLL circuit which has the voltage controlled oscillator which outputs the aforementioned feedback signal with which oscillation frequency was changed according to the voltage level of the aforementioned control signal. That the aforementioned control signal is more than a predetermined voltage level by furthermore, the 1st detection means to detect and this 1st detection means When it is detected that the aforementioned control signal is more than a predetermined voltage level That the aforementioned feedback signal is not oscillating by the 2nd detection means to detect and this 2nd detection means When it is detected that the aforementioned feedback signal is not oscillating, the PLL circuit characterized by having the 3rd detection means which outputs the detecting signal for lowering the voltage level of the aforementioned control signal is offered.

[0014] Here, the aforementioned detecting signal is inputted into the aforementioned charge pump,

and, as for the aforementioned charge pump, it is desirable to output the aforementioned error signal for lowering the voltage level of the aforementioned control signal according to the aforementioned detecting signal. Moreover, it is the above-mentioned PLL circuit and it is desirable to have further the means which lowers the voltage level of the aforementioned control signal according to the aforementioned detecting signal.

[0015]

[Embodiments of the Invention] Below, based on the suitable example shown in an attached drawing, the PLL circuit of this invention is explained in detail.

[0016] First, drawing 1 is the conceptual diagram of one example of the PLL circuit of this invention. Like the conventional PLL circuit 30 shown in drawing 4 , the PLL circuit 10 of the example of illustration has a phase comparator 12, the charge pump 14, a low pass filter 16, and a voltage controlled oscillator 18, and has the control circuit 20 further. Moreover, the control circuit 20 is constituted by the Schmidt type buffer 22, the flip-flop 24, and the combinational circuit 26 in the example of illustration.

[0017] In this PLL circuit 10, the reference signal supplied from the exterior of the PLL circuit 10 and the feedback signal outputted from a voltage controlled oscillator 18 are inputted into the phase comparator 12. In a phase comparator 12, the phase contrast between a reference signal and a feedback signal is detected, and the control signal which it is as a result of [the] a phase comparison is outputted from a phase comparator 12.

[0018] The control signal outputted from a phase comparator 12 and the detecting signal outputted from a control circuit 20 are inputted into the charge pump 14. From the charge pump 14, an error signal which will lower the voltage level of a control signal if a detecting signal is an active state is outputted, and if a detecting signal is in an inactive state, according to the control signal outputted from a phase comparator 12, the error signal which has the pulse width according to the phase contrast between a reference signal and a feedback signal will be outputted.

[0019] Moreover, the error signal outputted from the charge pump 14 is inputted into the low pass filter 16. In a low pass filter 16, an error signal is changed into an analog signal and the control signal which has a voltage level according to the error signal is outputted from a low pass filter 16.

[0020] The control signal outputted from a low pass filter 16 is inputted into the voltage controlled oscillator 18. In a voltage controlled oscillator 18, according to the voltage level of a control signal, the oscillation frequency of a feedback signal and the output signal of this PLL circuit 10 is changed, and the feedback signal with which oscillation frequency was changed, and the output signal of this PLL circuit 10 are outputted from a voltage controlled oscillator 18.

[0021] The control signal outputted from a low pass filter 16 and the feedback signal outputted from a voltage controlled oscillator 18 are inputted into the control circuit 20. In a control circuit 20, the voltage level of a control signal is detected, it is detected whether the PLL circuit 10 is in a deadlock state, and from a control circuit 20, if the PLL circuit 10 is in a deadlock state, in order to return this to a normal lock state, the detecting signal of an active state is outputted.

[0022] Here, a control signal is inputted into the Schmidt type buffer 22, and the output is inputted into the clear input terminal of a flip-flop 24, and one input terminal of a combinational circuit 26. Moreover, the data input terminal D of a flip-flop 24 is connected to a power supply, and the feedback signal is inputted into the clocked-into terminal. The input terminal of another side of a combinational circuit 26 is connected to the output terminal Q of a flip-flop 24, and the detecting signal which is the output signal is inputted into the charge pump 14.

[0023] In addition, although the detecting signal outputted from a control circuit 20 is inputted into the charge pump 14, and it is made to make the error signal for lowering the voltage level of a control signal output when this detecting signal is an active state, a detecting signal may be inputted into the

gate of an N type MOS transistor where it was not limited only to this example, for example, the drain was connected to the control signal, and the source was connected to the gland, and a means which carries out the direct discharge of the voltage level of a control signal may be

[0024] Moreover, although the Schmidt type buffer 22 is used in the above-mentioned example in order to detect the voltage level of a control signal, it is not limited to this, for example, the circuit using the AD converter can also be used. moreover, other combinational circuits which realize an equivalent function, for example although the flip-flop 24 and the combinational circuit 26 are used in order to generate a detecting signal -- or a control signal is also generable with microcomputer control etc.

[0025] Thus, what is necessary is not to limit especially the composition of a control circuit 20, but just to make it into the circuitry which outputs a detecting signal so that the voltage level of a control signal can be lowered in the design stage, in the PLL circuit of this invention, when the voltage level of the control signal with which a PLL circuit may be in a deadlock state is detected and a PLL circuit lapses into a deadlock state from the oscillation frequency characteristic of a voltage controlled oscillator. The PLL circuit of this invention is constituted as mentioned above fundamentally.

[0026] Next, operation of the PLL circuit of this invention is explained. First, the voltage level of a control signal explains operation in the case of being below the voltage level from which the PLL circuit 10 will be in a normal lock state.

[0027] In a control circuit 20, when the voltage level of a control signal is below a voltage level beforehand set up by the design stage, the output of the Schmidt type buffer 22 is a low level, therefore a detecting signal is the low level of an inactive state. In the PLL circuit 10 of the example of illustration, first, in a phase comparator 12, the phase contrast between a reference signal and a feedback signal is detected, and the control signal which it is as a result of [the] detection is outputted.

[0028] The control signal outputted from the phase comparator 12 is inputted into the charge pump 14, and the pulse which has the pulse width according to the phase contrast between a reference signal and a feedback signal as an error signal is outputted from the charge pump 14. The error signal outputted from the charge pump 14 is inputted into a low pass filter 16, it is changed into an analog signal by the low pass filter 16 according to the filter constant, and the control signal which has a predetermined voltage level is outputted.

[0029] The control signal outputted from the low pass filter 16 is inputted into a voltage controlled oscillator 18, and the oscillation frequency of the feedback signal and output signal which were outputted from the voltage controlled oscillator 18 is changed according to the voltage level of this control signal. And the frequency and the phase of a reference signal and an output signal synchronize by repeating and comparing a reference signal with the feedback signal with which oscillation frequency was changed similarly hereafter (lock).

[0030] The PLL circuit of this invention operates as mentioned above fundamentally. Next, the voltage level of a control signal explains operation at the time of becoming more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state, referring to the timing chart shown in drawing 2 and drawing 3 . In addition, in the timing chart of the example of illustration, the same sign as the signals A and B shown in drawing 1 is used.

[0031] Operation of the PLL circuit 10 becomes unstable, the voltage level of a control signal goes up, and when the high-level threshold Vih of the Schmidt type buffer 22 beforehand set up in the design stage is exceeded, high level is outputted from the Schmidt type buffer 22. That is, it is detected that the voltage level of a control signal became with the Schmidt type buffer 22 more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state.

[0032] At this time, a clearance is canceled, and a flip-flop 24 is made into operating state, and let a

combinational circuit 26 be operating state similarly.

[0033] As shown in the timing chart of drawing 2 , when the feedback signal has not toggled here, a clock signal is not inputted into a flip-flop 24, but the output Q is in a state with the cleared low level. The low level of the output Q of a flip-flop 24 is reversed by the combinational circuit 26, and a detecting signal changes to the high level which is an active state. That is, it is detected that the PLL circuit 10 has lapsed into the deadlock state.

[0034] If a detecting signal becomes high-level, from the charge pump 14, an error signal which lowers the oscillation frequency of a control signal will be outputted. Thereby, the voltage level of the control signal outputted from a low pass filter 16 falls gradually, and the oscillation frequency of a voltage controlled oscillator 18 falls, consequently a feedback signal starts a toggle again.

[0035] If a feedback signal starts a toggle, a clock signal will be inputted into a flip-flop 24, the output Q will become high-level, and a detecting signal will be returned to the low level which is in an inactive state. And in a phase comparator 12, a reference signal is compared with a feedback signal and the oscillation frequency of a voltage controlled oscillator 18 is repeatedly changed through the charge pump 14 and a low pass filter 16.

[0036] Here, if the voltage level of a control signal falls and it becomes smaller than the threshold of the low level of the Schmidt type buffer 22, the output of the Schmidt type buffer 22 is set to a low level, by this, a flip-flop 24 is cleared, the output Q is set to a low level, and a combinational circuit 26 will also be made into an inoperative state, and will be returned to an initial state. Similarly hereafter, a reference signal is repeatedly compared with a feedback signal, and, finally the frequency and the phase of a reference signal and an output signal synchronize.

[0037] Thus, in the PLL circuit of this invention, even if it is the case where the PLL circuit 10 lapses into a deadlock state, it detects that the voltage level of a control signal became more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state, and it can detect that the PLL circuit 10 has lapsed into the deadlock state further, and it can be automatically returned to a normal lock state.

[0038] On the other hand, when it does not lapse into a deadlock state in fact but the feedback signal has toggled even if that the voltage level of a control signal became more than the voltage level from which the PLL circuit 10 may be in a deadlock state is the case where it is detected as shown in the timing chart of drawing 3 , a clock signal is inputted into a flip-flop 24, the output Q changes high-level and a detecting signal holds the low level which is in an inactive state.

[0039] Therefore, like the time of normal operation, a reference signal is repeatedly compared with a feedback signal, the oscillation frequency of a voltage controlled oscillator 18 is changed, and, finally the frequency and the phase of a reference signal and an output signal synchronize.

[0040] Thus, in the PLL circuit of this invention, even if the voltage level of a control signal is the case where it becomes more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state, when having not actually lapsed into a deadlock state, normal operation is not affected at all.

[0041]

[Effect of the Invention] As explained to the detail above, the PLL circuit of this invention detects that the voltage level of a control signal became more than the voltage level by which a PLL circuit may lapse into a deadlock state, detects that the PLL circuit has lapsed into the deadlock state further, reduces the voltage level of a control signal, and it is constituted so that a PLL circuit may be returned to a normal lock state. For this reason, since it can be made to return to a normal lock state automatically according to the PLL circuit of this invention even if it is the case where it lapses into a deadlock state, the stable PLL circuit system can be built.

[Translation done.]

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TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the PLL circuit (Phase-Locked Loop : phase synchronous loop) which generates the output signal by which phase simulation was carried out to the reference signal.

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* NOTICES *

PRIOR ART

[Description of the Prior Art] Drawing 4 is the conceptual diagram of an example showing the internal configuration of a PLL circuit. The PLL circuit 30 of the example of illustration is constituted by the voltage controlled oscillator 38 which outputs a feedback signal and an output signal according to the voltage level of the phase comparator 32 which compares the phase of a reference signal and a feedback signal and outputs a control signal, the charge pump 34 which outputs an error signal according to a control signal, the low pass filter 36 which outputs the control signal which has a voltage level according to the error signal, and a control signal.

[0003] In this PLL circuit 30, in a phase comparator 32, the phase contrast between a reference signal and a feedback signal is detected, and the control signal which it is as a result of [the] comparison is outputted. An error signal is generated based on a control signal, after an error signal is changed into an analog signal by the low pass filter 36, it is inputted into a voltage controlled oscillator 38 as a control signal by the charge pump 34, and the oscillation frequency of a feedback signal is changed in a voltage controlled oscillator 38 with it according to the voltage level of this control signal.

[0004] For example, when the phase of a feedback signal is later, in order to carry out the phase of a feedback signal early to a reference signal, it is made high, and the voltage level of a control signal is conversely made low in a voltage level, when early. And by repeating and detecting similarly hereafter the phase contrast between a reference signal and the feedback signal with which oscillation frequency was changed, the frequency and the phase between a reference signal and a feedback signal were synchronized (lock), and the output signal has been obtained.

[0005] Thus, in the PLL circuit 30, the frequency and the phase of a feedback signal were controlled by the voltage level of a control signal, and the output signal with which the phase of a reference signal and a feedback signal synchronized has been obtained by it.

[0006] By the way, the above-mentioned PLL circuit 30 is carried in individual ICs, such as a control unit, a processor, and CPU, turns on chip, and it is not only IC-ized alone, but may be used for the clock control etc. In this case, if various conditions, such as voltage variation, and temperature change, process change, are taken into consideration, it is necessary to design a voltage controlled oscillator 38 with sufficient margin so that it can operate from low frequency to high frequency focusing on the oscillation frequency used.

[0007] Thus, in IC in which the PLL circuit 30 designed with sufficient margin for the oscillation frequency of a voltage controlled oscillator 38 is carried, a voltage controlled oscillator 38 can be oscillated to very high frequency rather than the real frequency of operation when actually operating IC. For example, though it does not oscillate to so high frequency at the time of worst conditions, at the time of best conditions, the maximum oscillation frequency of a voltage controlled oscillator 38 turns into typical conditions and very high frequency further.

[0008] By the way, circuit elements, such as a logic gate and a flip-flop, are usually connected to the

path of a feedback signal. However, if the operating state of the PLL circuit 30 becomes unstable, the voltage level of a control signal goes up and the oscillation frequency of a voltage controlled oscillator 38 becomes high, it becomes impossible for one on the path of a feedback signal of circuit elements to toggle on the oscillation frequency of a voltage controlled oscillator 38, and a feedback signal may not no longer be inputted into a phase comparator 32.

[0009] If a feedback signal is no longer inputted into a phase comparator 32, it will judge that the phase comparator 32 is behind a reference signal in a feedback signal, and the control signal for making high further oscillation frequency of a voltage controlled oscillator 38 will be outputted. thus, the voltage level of a control signal goes up further -- having -- just -- being alike -- it changes a stack into a state with a high voltage level, and lapses into the deadlock state where the oscillation frequency of a voltage controlled oscillator 38 is fixed to an oscillation upper limited frequency

[0010] However, if the PLL circuit 30 did not initialize making a power supply into an OFF state, for example etc. once it lapsed into the deadlock state, it was difficult for constituting the PLL circuit system which could not be returned to a normal lock state and stabilized.

[0011] Therefore, in IC in which the PLL circuit 30 was carried, in order to avoid a deadlock state beforehand, in consideration of the upper limited frequency of the path of a feedback signal of operation, you have to design so that it can operate to frequency very higher than the real frequency of operation of IC. When the PLL circuit 30 was especially used for clock control, the restrictions on a design -- the path of a clock signal must enable it to operate to frequency very higher than a real frequency of operation, and the restrictions to the load of the path of a clock signal become severe -- increased, and there was a trouble that a design became very difficult.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained to the detail above, the PLL circuit of this invention detects that the voltage level of a control signal became more than the voltage level by which a PLL circuit may lapse into a deadlock state, detects that the PLL circuit has lapsed into the deadlock state further, reduces the voltage level of a control signal, and it is constituted so that a PLL circuit may be returned to a normal lock state. For this reason, since it can be made to return to a normal lock state automatically according to the PLL circuit of this invention even if it is the case where it lapses into a deadlock state, the stable PLL circuit system can be built.

[Translation done.]

* NOTICES *

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The purpose of this invention tries to return the trouble based on the aforementioned conventional technology, detects having lapsed into the deadlock state, and is to offer the PLL circuit which can return to a normal state automatically.

[Translation done.]

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MEANS

[Means for Solving the Problem] The phase comparator which this invention detects the phase contrast between a reference signal and a feedback signal, and outputs a control signal in order to attain the above-mentioned purpose, The charge pump which outputs the error signal which has the pulse width according to the phase contrast between the aforementioned reference signal and a feedback signal according to the aforementioned control signal, The low pass filter which outputs the control signal which has a voltage level according to the aforementioned error signal, It is the PLL circuit which has the voltage controlled oscillator which outputs the aforementioned feedback signal with which oscillation frequency was changed according to the voltage level of the aforementioned control signal. That the aforementioned control signal is more than a predetermined voltage level by furthermore, the 1st detection means to detect and this 1st detection means When it is detected that the aforementioned control signal is more than a predetermined voltage level That the aforementioned feedback signal is not oscillating by the 2nd detection means to detect and this 2nd detection means When it is detected that the aforementioned feedback signal is not oscillating, the PLL circuit characterized by having the 3rd detection means which outputs the detecting signal for lowering the voltage level of the aforementioned control signal is offered.
[0014] Here, the aforementioned detecting signal is inputted into the aforementioned charge pump, and, as for the aforementioned charge pump, it is desirable to output the aforementioned error signal for lowering the voltage level of the aforementioned control signal according to the aforementioned detecting signal. Moreover, it is the above-mentioned PLL circuit and it is desirable to have further the means which lowers the voltage level of the aforementioned control signal according to the aforementioned detecting signal.
[0015]
[Embodiments of the Invention] Below, based on the suitable example shown in an attached drawing, the PLL circuit of this invention is explained in detail.
[0016] First, drawing 1 is the conceptual diagram of one example of the PLL circuit of this invention. Like the conventional PLL circuit 30 shown in drawing 4 , the PLL circuit 10 of the example of illustration has a phase comparator 12, the charge pump 14, a low pass filter 16, and a voltage controlled oscillator 18, and has the control circuit 20 further. Moreover, the control circuit 20 is constituted by the Schmidt type buffer 22, the flip-flop 24, and the combinational circuit 26 in the example of illustration.
[0017] In this PLL circuit 10, the reference signal supplied from the exterior of the PLL circuit 10 and the feedback signal outputted from a voltage controlled oscillator 18 are inputted into the phase comparator 12. In a phase comparator 12, the phase contrast between a reference signal and a feedback signal is detected, and the control signal which it is as a result of [the] a phase comparison is outputted from a phase comparator 12.

[0018] The control signal outputted from a phase comparator 12 and the detecting signal outputted from a control circuit 20 are inputted into the charge pump 14. From the charge pump 14, an error signal which will lower the voltage level of a control signal if a detecting signal is an active state is outputted, and if a detecting signal is in an inactive state, according to the control signal outputted from a phase comparator 12, the error signal which has the pulse width according to the phase contrast between a reference signal and a feedback signal will be outputted.
[0019] Moreover, the error signal outputted from the charge pump 14 is inputted into the low pass filter 16. In a low pass filter 16, an error signal is changed into an analog signal and the control signal which has a voltage level according to the error signal is outputted from a low pass filter 16.
[0020] The control signal outputted from a low pass filter 16 is inputted into the voltage controlled oscillator 18. In a voltage controlled oscillator 18, according to the voltage level of a control signal, the oscillation frequency of a feedback signal and the output signal of this PLL circuit 10 is changed, and the feedback signal with which oscillation frequency was changed, and the output signal of this PLL circuit 10 are outputted from a voltage controlled oscillator 18.
[0021] The control signal outputted from a low pass filter 16 and the feedback signal outputted from a voltage controlled oscillator 18 are inputted into the control circuit 20. In a control circuit 20, the voltage level of a control signal is detected, it is detected whether the PLL circuit 10 is in a deadlock state, and from a control circuit 20, if the PLL circuit 10 is in a deadlock state, in order to return this to a normal lock state, the detecting signal of an active state is outputted.
[0022] Here, a control signal is inputted into the Schmidt type buffer 22, and the output is inputted into the clear input terminal of a flip-flop 24, and one input terminal of a combinational circuit 26. Moreover, the data input terminal D of a flip-flop 24 is connected to a power supply, and the feedback signal is inputted into the clocked-into terminal. The input terminal of another side of a combinational circuit 26 is connected to the output terminal Q of a flip-flop 24, and the detecting signal which is the output signal is inputted into the charge pump 14.
[0023] In addition, although the detecting signal outputted from a control circuit 20 is inputted into the charge pump 14, and it is made make the error signal for lowering the voltage level of a control signal output when this detecting signal is an active state, a detecting signal may be inputted into the gate of an N type MOS transistor where it was not limited only to this example, for example, the drain was connected to the control signal, and the source was connected to the gland, and a means which carries out the direct discharge of the voltage level of a control signal may be established
[0024] Moreover, although the Schmidt type buffer 22 is used in the above-mentioned example in order to detect the voltage level of a control signal, it is not limited to this, for example, the circuit using the AD converter can also be used. moreover, other combinational circuits which realize an equivalent function, for example although the flip-flop 24 and the combinational circuit 26 are used in order to generate a detecting signal -- or a control signal is also generable with microcomputer control etc.
[0025] Thus, what is necessary is not to limit especially the composition of a control circuit 20, but just to make it into the circuitry which outputs a detecting signal so that the voltage level of a control signal can be lowered in the design stage, in the PLL circuit of this invention, when the voltage level of the control signal with which a PLL circuit may be in a deadlock state is detected and a PLL circuit lapses into a deadlock state from the oscillation frequency characteristic of a voltage controlled oscillator. The PLL circuit of this invention is constituted as mentioned above fundamentally.
[0026] Next, operation of the PLL circuit of this invention is explained. First, the voltage level of a control signal explains operation in the case of being below the voltage level from which the PLL circuit 10 will be in a normal lock state.
[0027] In a control circuit 20, when the voltage level of a control signal is below a voltage level beforehand set up by the design stage, the output of the Schmidt type buffer 22 is a low level,

therefore a detecting signal is the low level of an inactive state. In the PLL circuit 10 of the example of illustration, first, in a phase comparator 12, the phase contrast between a reference signal and a feedback signal is detected, and the control signal which it is as a result of [the] detection is outputted.

[0028] The control signal outputted from the phase comparator 12 is inputted into the charge pump 14, and the pulse which has the pulse width according to the phase contrast between a reference signal and a feedback signal as an error signal is outputted from the charge pump 14. The error signal outputted from the charge pump 14 is inputted into a low pass filter 16, it is changed into an analog signal by the low pass filter 16 according to the filter constant, and the control signal which has a predetermined voltage level is outputted.

[0029] The control signal outputted from the low pass filter 16 is inputted into a voltage controlled oscillator 18, and the oscillation frequency of the feedback signal and output signal which were outputted from the voltage controlled oscillator 18 is changed according to the voltage level of this control signal. And the frequency and the phase of a reference signal and an output signal synchronize by repeating and comparing a reference signal with the feedback signal with which oscillation frequency was changed similarly hereafter (lock).

[0030] The PLL circuit of this invention operates as mentioned above fundamentally. Next, the voltage level of a control signal explains operation at the time of becoming more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state, referring to the timing chart shown in drawing 2 and drawing 3 . In addition, in the timing chart of the example of illustration, the same sign as the signals A and B shown in drawing 1 is used.

[0031] Operation of the PLL circuit 10 becomes unstable, the voltage level of a control signal goes up, and when the high-level threshold Vih of the Schmidt type buffer 22 beforehand set up in the design stage is exceeded, high level is outputted from the Schmidt type buffer 22. That is, it is detected that the voltage level of a control signal became with the Schmidt type buffer 22 more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state.

[0032] At this time, a clearance is canceled, and a flip-flop 24 is made into operating state, and let a combinational circuit 26 be operating state similarly.

[0033] As shown in the timing chart of drawing 2 , when the feedback signal has not toggled here, a clock signal is not inputted into a flip-flop 24, but the output Q is in a state with the cleared low level. The low level of the output Q of a flip-flop 24 is reversed by the combinational circuit 26, and a detecting signal changes to the high level which is an active state. That is, it is detected that the PLL circuit 10 has lapsed into the deadlock state.

[0034] If a detecting signal becomes high-level, from the charge pump 14, an error signal which lowers the oscillation frequency of a control signal will be outputted. Thereby, the voltage level of the control signal outputted from a low pass filter 16 falls gradually, and the oscillation frequency of a voltage controlled oscillator 18 falls, consequently a feedback signal starts a toggle again.

[0035] If a feedback signal starts a toggle, a clock signal will be inputted into a flip-flop 24, the output Q will become high-level, and a detecting signal will be returned to the low level which is in an inactive state. And in a phase comparator 12, a reference signal is compared with a feedback signal and the oscillation frequency of a voltage controlled oscillator 18 is repeatedly changed through the charge pump 14 and a low pass filter 16.

[0036] Here, if the voltage level of a control signal falls and it becomes smaller than the threshold of the low level of the Schmidt type buffer 22, the output of the Schmidt type buffer 22 is set to a low level, by this, a flip-flop 24 is cleared, the output Q is set to a low level, and a combinational circuit 26 will also be made into an inoperative state, and will be returned to an initial state. Similarly hereafter, a reference signal is repeatedly compared with a feedback signal, and, finally the frequency

and the phase of a reference signal and an output signal synchronize.

[0037] Thus, in the PLL circuit of this invention, even if it is the case where the PLL circuit 10 lapses into a deadlock state, it detects that the voltage level of a control signal became more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state, and it can detect that the PLL circuit 10 has lapsed into the deadlock state further, and it can be automatically returned to a normal lock state.

[0038] On the other hand, when it does not lapse into a deadlock state in fact but the feedback signal has toggled even if that the voltage level of a control signal became more than the voltage level from which the PLL circuit 10 may be in a deadlock state is the case where it is detected as shown in the timing chart of drawing 3 , a clock signal is inputted into a flip-flop 24, the output Q changes high-level and a detecting signal holds the low level which is in an inactive state.

[0039] Therefore, like the time of normal operation, a reference signal is repeatedly compared with a feedback signal, the oscillation frequency of a voltage controlled oscillator 18 is changed, and, finally the frequency and the phase of a reference signal and an output signal synchronize.

[0040] Thus, in the PLL circuit of this invention, even if the voltage level of a control signal is the case where it becomes more than the voltage level by which the PLL circuit 10 may lapse into a deadlock state, when having not actually lapsed into a deadlock state, normal operation is not affected at all.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the conceptual diagram of one example of the PLL circuit of this invention.
[Drawing 2] It is the timing chart showing operation of the PLL circuit of this invention of one example.
[Drawing 3] It is the timing chart showing operation of the PLL circuit of this invention of another example.
[Drawing 4] It is the conceptual diagram of an example of a PLL circuit.
[Description of Notations]
10 30 PLL circuit
12 32 Phase comparator
14 34 Charge pump
16 36 Low pass filter
18 38 Voltage controlled oscillator
20 Control Circuit
22 Schmidt Type Buffer
24 Flip-flop
26 Combinational Circuit

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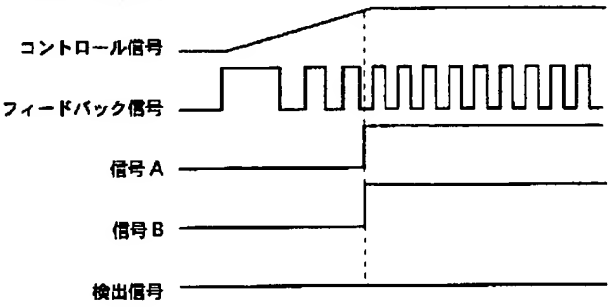
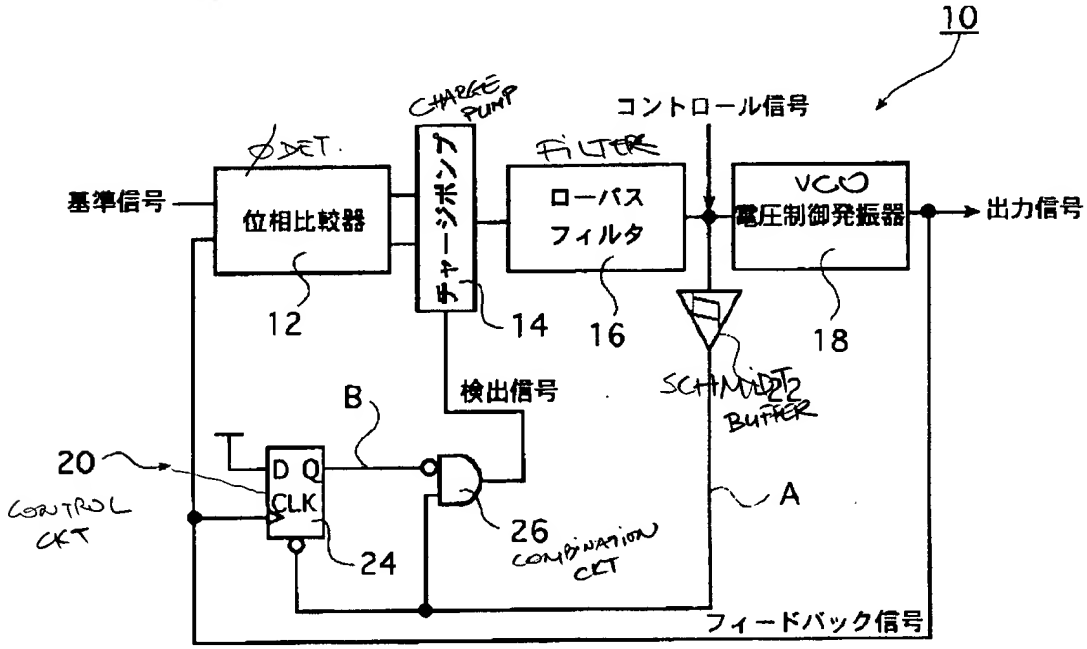
DRAWINGS

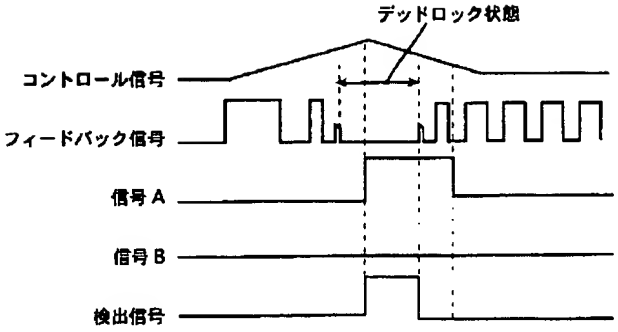
[Drawing 3]



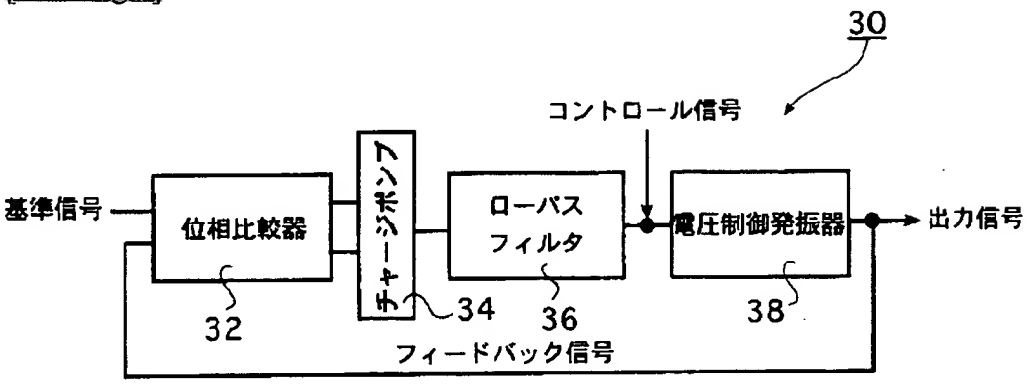
[Drawing 1]



[Drawing 2]



[Drawing 4]



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